CLAIMS

1. An integrated circuit having:

at least one external connection pin, the pin being coupled to a pad cell adapted to provide a signal path from circuitry external to the integrated circuit via the pin to components of the integrated circuit, and wherein the pad cell includes a first signal path being operational under a first set of normal operating conditions and a second signal path, the second signal path being non-operable under the first set of normal operating conditions and operable on application of a pre-defined signal to the pin, the operation of the second signal path being parallel to and simultaneous with the operation of the first signal path.

2. The circuit as claimed in claim 1 wherein the second signal path includes a MOS transistor device, the source and well of the device being coupled to one another.

3. The circuit as claimed in claim 2 wherein the source and well are coupled to the pin.

4. The circuit as claimed in claim 2 wherein the second signal path additional includes comparator circuitry.

5. The circuit as claimed in claim 4 wherein the comparator circuitry includes a digital gate.

6. The circuit as claimed in claim 4 wherein the comparator circuitry includes an analog amplifier.

7. The circuit as claimed in claim 6 wherein the amplifier is configured as an inverter.

8. The circuit as claimed in claim 4 wherein the comparator circuitry is coupled in series to a first MOS device.

9. The circuit as claimed in claim 4 wherein the second signal path is additionally coupled to an impedance device such that when the second signal path is operable, the pin

sources current through the MOS device across the impedance, thereby causing the comparator circuitry to change its output.

10. The circuit as claimed in claim 9 wherein the impedance device is an active component.

11. The circuit as claimed in claim 9 wherein the impedance device is a passive component.

12. The circuit as claimed in claim 1 wherein the second signal path may be replicated such that the pad cell provides multiple signal paths that may be operable simultaneously with and in parallel to the first signal path.

13. The circuit as claimed in claim 12 wherein each of the multiple signal paths of the pad cell are individually operable such that at any one time only one signal path of the multiple signal paths is operable.

14. The circuit as claimed in claim 1 wherein the pre-defined signal is a signal of larger magnitude than the first set of normal operating conditions.

15. The circuit as claimed in claim 4 wherein the comparator circuitry includes a first input coupled to the MOS device, a second input adapted to provide a signal with which the signal coupled from the MOS device is compared with and an output, the output depending on the comparison effected between the first and second inputs.

16. The circuit as claimed in claim 15 wherein the comparator circuitry is configured as a current comparator.

17. The circuit as claimed in claim 15 wherein the comparator circuitry is configured as a voltage comparator.

18. The circuit as claimed in claim 15 wherein an analog filter is provided between the MOS device and the comparator circuitry.

19. The circuit as claimed in claim 15 wherein a digital filter is provided at the output of the comparator circuitry.

20. The circuit as claimed in claim 15 wherein the comparator circuitry is configured as a SAR ADC.

21. The circuit as claimed in claim 15 wherein the comparator circuitry is configured as a flash ADC.

22. The circuit as claimed in claim 15 further comprising at least one additional MOS device provided in the path between the first MOS device and the input to the comparator circuitry.

23. The circuit as claimed in claim 1 wherein the first signal path includes an up/down diode configuration adapted to provide protection from electrostatic discharge events.

24. The circuit as claimed in claim 23 wherein the first signal path additionally includes an impedance element in series with the up/down diode configuration.

25. The circuit as claimed in claim 24 wherein the first signal path additionally includes a digital buffer in series with the up/down diode configuration.

26. An integrated circuit comprising:

internal circuitry,

at least one external connection,

a pad cell electrically interposed between an external connection and the internal circuitry, the pad cell comprising:

a first group of components adapted to protect the internal circuitry from transients at the external connection and providing, during normal operating conditions of the integrated circuit, a first signal path to the internal circuitry,

a second group of components providing a second signal path from the external connection to the internal circuitry and wherein the second signal path is non-

operable during the normal operating conditions but on application of a predefined voltage at the external connection becomes operable, the first and second signal paths being simultaneously operable.

27. The circuit as claimed in claim 26 wherein the second signal path includes a MOS device with the source and well coupled together, the gate of the MOS device being controllable by a control voltage, the MOS device being switchable between an off condition and an on condition, and wherein in the off condition the MOS device presents a high impedance to the external connection.

28. The circuit as claimed in claim 26 wherein the second group of components includes a comparator, the comparator adapted to compare a first signal applied at the external connection with a second signal and provide an output dependent on that comparison.

29. The circuit as claimed in claim 27 wherein the comparator is configured as a current comparator.

30. The circuit as claimed in claim 27 wherein the comparator is configured as a voltage comparator.

31. The circuit as claimed in claim 26 wherein the second group of components include at least one filter.

32. The circuit as claimed in claim 31 wherein the filter is an analog filter.

33. The circuit as claimed in claim 31 wherein the filter is a digital filter.

34. An integrated circuit comprising:

internal circuitry,

at least one external connection,

a pad cell electrically interposed between an external connection and the internal circuitry, the pad cell comprising:

a first group of components providing, during normal operating conditions of the integrated circuit, a first signal path to the internal circuitry,

a second group of components providing a second signal path from the external connection to the internal circuitry and wherein the second signal path is non-operable during the normal operating conditions but on application of a predefined voltage at the external connection becomes operable, the second group of components including a MOS device having the source and well coupled together, the application of the predefined voltage turning the MOS device on and enabling the second signal path.

35. The circuit as claimed in claim 34 wherein the pad cell further includes circuit components adapted to protect the internal circuitry from transients at the external connection.

36. The circuit as claimed in claim 35 wherein the circuit components adapted to protect the internal circuitry from transients at the external connection are provided in one or other of the first and second signal paths.

37. The circuit as claimed in claim 35 wherein the circuit components adapted to protect the internal circuitry from transients at the external connection are provided in the first signal path.

38. The circuit as claimed in claim 35 being configured such that during operation of the second signal path the first signal path in not operable.

39. The circuit as claimed in claim 38 wherein the first signal path is available for operation but is not operable.

40. The circuit as claimed in claim 38 wherein the first signal path is disabled.

41. The circuit as claimed in claim 35 wherein the second signal path includes components which may be configured to disable the second signal path.

42. The circuit as claimed in claim 41 wherein the second signal path may be permanently disabled.

43. The circuit as claimed in claim 34 further including components which may be configured to disable the second signal path during the application of the predetermined voltage at the external connection.

44. The circuit as claimed in claim 43 wherein the second signal path may be permanently disabled.